In the Claims

Claims 1-51 (cancelled)

Claim 52 (previously presented): An array of memory cells comprising:

a set of capacitor constructions, the set of capacitor constructions being defined to include a first subset of capacitor constructions and a second subset of capacitor constructions;

a first wordline over the set of capacitor constructions, the first wordline being in electrical connection with the first subset of capacitor constructions;

a second wordline over the first wordline and in electrical connection with the second subset of capacitor constructions; and

wherein the first wordline does not electrically connect with the second subset of capacitor constructions and the second wordline does not electrically connect with the first subset of capacitor constructions.

Claim 53 (previously presented): The array of claim 52 wherein the second wordline is over the set of capacitor constructions.

Claim 54 (previously presented): The array of claim 53 further comprising:

openings extending through the first wordline and proximate the second subset of capacitor constructions;

sidewall spacers within the openings and narrowing the openings; and

conductive material within the openings, the conductive material electrically connecting the second wordline to the second subset of capacitor constructions.

Claim 55 (previously presented): The array of claim 54 wherein the conductive material comprises conductively-doped silicon.

Claim 56 (previously presented): The array of claim 53 wherein the first and second wordlines comprise conductively-doped silicon.

Claim 57 (previously presented): The array of claim 53 further comprising an insulative material layer over the second subset of capacitor constructions; the insulative material layer physically and electrically separating the second subset of capacitor constructions from the first wordline.

Claim 58 (previously presented): The array of claim 57 wherein the insulative material layer comprises silicon nitride.

Claim 59 (previously presented): The array of claim 53 further comprising:

a semiconductive material over the set of capacitor constructions;

source/drain regions within the semiconductive material, the source/drain regions being proximate at least some of the first and second wordlines;

openings extending through the first and second wordlines and to the source/drain regions; and

bitline interconnections within the openings and electrically connected through the source/drain regions to the set of capacitor constructions.

Claims 60-72 (cancelled).